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FZ/DD

A device for sending/receiving digital data capable of processing different bit rates, in particular in a VDSL environment.

The invention relates generally to sending and receiving digital data that can have different bit rates, and more particularly to choosing the capacity of memory means used by interleaving and deinterleaving processes effected within send/receive devices capable of processing different bit rates.

The invention is advantageously applied to a VDSL (Very High Rate Digital Subscriber Line) environment or system, i.e. a digital communication system linking an operator and users via very high bit rate transmission lines. This application is not limiting on the invention.

Thus the invention applies more particularly to send/receive devices, usually referred to as "modems", at the operator and user ends of a transmission line.

The skilled person knows that a VDSL communication system is capable of delivering "symmetrical" services and "asymmetrical" services. A service is referred to as "symmetrical" if the bit rate of information exchanged between the operator and the user in both transmission directions (i.e. from the operator to the user and from the user to the operator) is exactly the same.

A service is referred to as "asymmetrical" if the bit rate of information sent in one transmission direction is different from the bit rate of information sent in the other transmission direction.

The processes of interleaving and deinterleaving data sent and received by a modem necessitates the use of memories. For a modem intended to operate at a predetermined bit rate, the memories must have a capacity that depends on that bit rate.

The invention aims to propose a send/receive device (modem) architecture which requires a reduced quantity of memory, which can be used at the operator end or at the user end (in other words, which is fully interchangeable between sending and receiving) and which is adaptable, in particular in terms of the memory capacity of the interleaving and deinterleaving means, to suit a number of different bit rates selected from a predetermined group of bit rates.

The invention therefore proposes in particular to use memory means whose size is optimized for a global (send + receive) bit rate, which can be shared between the interleaving means and the deinterleaving means, and whose memory allocation can be reconfigured in accordance with the bit rate actually processed by the send/receive device (modem).

The invention therefore proposes a device for sending/receiving digital data and capable of processing different bit rates from a group of predetermined bit rates (for example all the symmetrical or asymmetrical services offered by the VDSL communication system).

The device according to the invention includes a coding/decoding stage (generally referred to by the skilled person as "channel coding/decoding stage") including interleaving means and deinterleaving means. The interleaving and deinterleaving means include a memory whose minimum size is fixed as a function of the maximum bit rate of said group (for example the highest asymmetrical bit rate in the case of a VDSL system). The memory also has a first memory space assigned to the interleaving means and a second memory space assigned to the deinterleaving means. The size of each of the two memory spaces is parameterable as a function of the bit rate actually processed by the device.

In the context of the present invention, the term

"bit rate" associated with a memory capacity or memory space is to be understood as being a global bit rate, i.e. the sum of the send and receive bit rates.

It is therefore possible to reduce considerably the size of the memory means required for the interleaving and deinterleaving means implemented within a modem that can be used either at the operator end or at the user end and which is capable of processing a number of different and symmetrical or asymmetrical bit rates.

The transmitted data stream is generally protected from transmission channel noise by a Reed-Solomon coding algorithm, well known to the skilled person. To make the Reed-Solomon coding more efficient, the coding means are coupled to the interleaving means so as to distribute in time errors introduced by the transmission channel, which often occur in bursts affecting several successive bytes, which can reduce the correction capacity of the Reed-Solomon code in isolation (generally eight bytes per packet). The interleaving means then interleave the bytes temporally by modifying the order in which they are transmitted, which achieves said temporal distribution of the errors.

To be more precise, in one embodiment of the invention, the channel coding/decoding stage includes Reed-Solomon coding/decoding means of length N (N = 240 bytes, for example). The interleaving means are then adapted to effect convolutional interleaving of I branches with $\underline{i} - 1$ blocks of M bytes. The deinterleaving means are adapted to implement convolutional deinterleaving with I' branches of $i' - 1$ blocks of M' bytes. I and I' are sub-multiples of N and $\underline{i}$ and i' are the current relative indexes of the branches. The size in bytes of the first memory space is equal to $I \times (I - 1) \times M/2$ and the size in bytes of the second memory space is equal to $I' \times (I' - 1) \times M'/2$. The sizes

of the two memory spaces are parameterable by I, I', M and M'.

Using convolutional triangular interleaving (and consequently convolutional triangular deinterleaving), instead of some other conventional type of interleaving, is particularly beneficial because it reduces latency generated by the memory. Convolutional triangular interleaving requires a much smaller memory, which reduces latency. Latency is a primordial and decisive criterion for any VDSL communication system.

In one particularly simple embodiment of the invention the memory is a random access memory, in particular a dual-port memory. The interleaving means and the deinterleaving means respectively include first addressing means and second addressing means. The first and second addressing means each include:

a first counter defining the relative index i or i' of a branch,

a second counter defining the number of bytes in a block and incremented each time that the first counter reaches its counting limit value,

a third counter defining the current index of a block in the branch with index i or i' and incremented each time that a block contains M or M' bytes, and

intermediate calculation means calculating the address of each branch in said memory from the content of the first counter.

The first addressing means further include first address determination means adapted to determine successive read and write addresses in said memory of data successively delivered to the interleaving means. The first address determination means determine said addresses from values supplied by the intermediate calculation means, the second and third counters and the parameter M.

The second addressing means further include second address determination means adapted to determine successive read and write addresses in said memory of data successively delivered to the deinterleaving means. The second address determination means determine said addresses from values supplied by the intermediate calculation means, the second and third counters, the parameter M' and the size of the first memory space (so that the first unoccupied address in the memory can be determined).

Other advantages and features of the invention will become apparent on examining the following detailed description of non-limiting embodiments of the invention and the accompanying drawings, in which:

- figure 1 is a highly diagrammatic representation of a communication system in accordance with the invention linking two send/receive devices;
- figure 2 shows diagrammatically and in more detail the internal architecture of a send/receive device according to the invention;
- figure 3 shows diagrammatically and in more detail the internal architecture of a coding/decoding stage of the device shown in figure 2;
- figures 4 and 5 show diagrammatically the theory of convolutional triangular interleaving and deinterleaving;
- figure 6 shows diagrammatically and in more detail the internal architecture of the interleaving and deinterleaving means of a send/receive device according to the invention;
- figure 7 shows diagrammatically one embodiment of first addressing means associated with the interleaving means; and
- figure 8 shows diagrammatically one embodiment of second addressing means associated with the

deinterleaving means.

An application of the invention to a VDSL communication system will now be described, although the invention is not limited to that application.

Thus figure 1 shows two send/receive devices TO and TU according to the invention, referred to more simply as terminals or modems. One of these terminals, for example the terminal TO, is at the operator end, and the other terminal TU is at the user end. The two modems are linked by a very high bit rate communication line LH.

The VDSL communication system enables the operator to provide symmetrical services, typically six symmetrical services S1-S6, i.e. services in which the information bit rates in the two transmission directions (from the operator to the user and from the user to the operator) are exactly the same. The service S1 with the lowest bit rate has a bit rate of 32 × 64 kbit/s, for example, and the fastest symmetrical service S6 has a bit rate of 362 × 64 kbit/s.

With the VDSL system, the operator can also provide "asymmetrical" services A1 - A6, i.e. services with different information bit rates in the user to operator direction (uplink direction) and in the operator to user direction (downlink direction).

The first asymmetrical service A1 has a bit rate in the uplink direction of 32 × 64 kbit/s, for example, and a bit rate in the downlink direction of 100 × 64 kbit/s.

The asymmetrical service having the highest global information bit rate (uplink bit rate + downlink bit rate) is the service A6, whose bit rate in the uplink direction is equal to 32 × 64 kbit/s and whose bit rate in the downlink direction is equal to 832 × 64 kbit/s.

The send/receive device according to the invention can therefore be installed at the user end or at the operator end and is capable of processing all the above

services, as described in more detail hereinafter, subject to choosing the capacity of the memory assigned to the interleaving/deinterleaving means in accordance with the maximum bit rate of the services offered, here the bit rate of the highest asymmetrical service (service A6), and provided that the parameters of the memory space of that memory are set in accordance with the service actually processed by the device.

The internal architecture of the operator terminal TO from figure 1 will now be described in more detail, and it is to be understood that everything described hereinafter is equally valid for the terminal TU.

The terminal TO includes a send system and a receive system both connected to the transmission line LH (see figure 2).

The terminal TO includes a channel coding/decoding stage ETC including a channel coding unit CC in the send system and a channel decoding unit DCC in the receive system.

The channel coding unit CC includes Reed-Solomon coding means whose structure and function are well known to the skilled person. The Reed-Solomon coding means are associated with interleaving means.

In conjunction with subsequent interleaving, the Reed-Solomon coding can correct bursts of errors introduced by the transmission channel. Reed-Solomon coding is applied individually to each of the data packets delivered to the input of the coding unit CC. Reed-Solomon coding adds a number of parity bytes to the bytes of the packets received and can therefore correct a number of erroneous bytes. It is assumed here, by way of example, that the Reed-Solomon code used is an RS (240, 224) code with a correcting power of 8. This notation means that the Reed-Solomon coding means are applied to packets of 224 bytes, to which they add 16

parity bytes, to form a Reed-Solomon coded word whose length is 240 bytes, which makes it possible to correct up to eight erroneous bytes.

In order to distribute temporally errors introduced by the channel, which often occur in bursts affecting several successive bytes and can therefore exceed the correction capacity of the Reed-Solomon code in isolation, the bytes are temporally interleaved by modifying the order in which they are transmitted. This improves the efficacy of the Reed-Solomon coding.

The information delivered to the output of the channel coding stage ETC is delivered to a modulation unit BM whose structure is known in the art and which effects quadrature modulation, for example. Then, after various standard processes have been effected in a send unit EM including in particular an interface to the transmission line LH, the modulated signal is transmitted over the transmission line LH.

Similarly, the receive system of the terminal TO includes at its input a receive unit ER including in particular a receive interface to the transmission line LH which effects standard processing. The modulated signal delivered to the output of the receive unit ER is demodulated in a demodulator unit BDM and the demodulated signal is then delivered to the channel decoding unit DCC. The latter unit includes in particular deinterleaving and Reed-Solomon decoding means.

The internal architecture and the operation of the interleaving and deinterleaving means will now be described in more detail with more particular reference to figures 3 *et seq*.

As shown in figure 3, and as already explained, the interleaving means MET follow the Reed-Solomon coding means CRS and the deinterleaving means MDET precede the Reed-Solomon decoding means DCRS.

As shown diagrammatically in figures 4 and 5, the interleaving and deinterleaving are convolutional triangular interleaving and deinterleaving with I branches of i - 1 blocks of M bytes for interleaving and I' branches of i' - 1 blocks of M' bytes for deinterleaving.

As explained in more detail hereinafter, the parameters I, M, I' and M' can be modified, for example by software, and are delivered by control means MCD (figure 3) which can take the form of software. These parameters define the sizes of the respective memory spaces assigned to the interleaving means and to the deinterleaving means according to the bit rate of the information sent by the terminal TO (parameters I and M) and the bit rate of the information received by the terminal TO (parameters I' and M').

The interleaving means therefore include I parallel branches BRi (numbered from 0 to I - 1, for example) which are implemented with a delay increment of M per branch (M represents the maximum number of bytes of a block BKj with index j). Each branch can be considered as a delay line, the length of the branch with index i, when i varies in the range from 0 to I - 1, being equal to $i \times M$ bytes. In figure 4, by way of example, I = 7.

Accordingly, the first block of M bytes (having the index 0, for example) is not interleaved and is delivered unmodified to the output of the interleaving means. The next block of M bytes (index 1) is delivered to the input of the branch BR1, and so on up to the seventh block of M bytes (index 6), which is delivered to the branch BR6. The cycle then begins again with the blocks of bytes with indices from 7 to 13, the preceding blocks of bytes being either delivered to the output of the interleaving means or moved forward by one block BKj in the branch concerned.

The deinterleaving means associated with the interleaving means MET, and which are consequently incorporated into the user terminal TU, have a structure analogous to that which has just been described for the interleaving means, but the indices of the branches are reversed so that the longest interleaving time-delay corresponds to the shortest deinterleaving time-delay.

The deinterleaving means MDET incorporated in the operator terminal TO have I' branches, the branch with index i' having a length equal to i' x M' bytes.

For simplicity, figure 5 represents the situation in which I' = I, but if the service is an asymmetrical service I and I' are generally different, of course, and likewise M and M'.

In hardware terms, as shown diagrammatically in figure 6, the interleaving means and the deinterleaving means include common memory means MM, for example a dual-port random access memory. The memory space of the memory MM is then divided into a first memory space ESM1 assigned to the interleaving means MET and a second memory space ESM2 assigned to the deinterleaving means MDET.

The interleaving means also include first addressing means MAD1 receiving the parameters I and M and the deinterleaving means also include second addressing means MAD2 receiving the parameters I' and M'. The structure of the addressing means is described in more detail hereinafter with reference to figures 7 and 8.

The minimum size of the memory MM is set by the maximum bit rate that the send/receive device can process. The maximum bit rate is, of course, the sum of the uplink bit rate and the downlink bit rate.

In this example the maximum bit rate is that of the largest asymmetrical service A6.

An example of the capacity of the memory MM and of the values chosen for the parameters I, M, I' and M' follows for an asymmetrical service A6 and an RS (240, 224) Reed-Solomon code with a correction power of 8 bytes/word, when the transmission lines are disturbed by an impulsive noise with a duration of 0.25 ms.

In the downlink direction, the maximum bit rate is equal to 832 × 64 kbit/s.

The number of bits affected by noise is consequently equal to the product of that bit rate by the duration of the impulsive noise, which yields a number of bits affected by noise equal to 13 312 (1 664 bytes). Given the correcting power of the Reed-Solomon code (here 8), the number nrs of Reed-Solomon words needed to correct 1 664 bytes subject to noise is equal to 1 664/8, i.e. 208.

The size of the memory space needed to store this maximum bit rate is then equal to N.nrs/2 where N is the size of the Reed-Solomon code (here 240).

The resulting memory space size is therefore equal to 24 960 bytes.

The bit rate in the uplink direction is equal to 32 × 64 kbit/s. A similar calculation shows that the number of bits affected by noise is equal to 512 and that nrs = 8. The memory size to be provided for the uplink direction is therefore equal to 1 920 bytes. The minimum size of the memory MM is therefore 26 880 bytes.

The parameters I, I', M and M' can be determined from the above capacities. To be more precise, the size of the first memory space needed to implement triangular convolutional interleaving with I branches of i-1 blocks of M bytes is equal to I × (I - 1) × M/2.

Similarly, the size of the second memory space ESM2 to support the uplink bit rate is equal to

$I' \times (I' - 1) \times M'/2$.

Also, I and I' must be sub-multiples of the size N of the Reed-Solomon code.

Since $I \times (I - 1) \times M/2$ must be equal to 24 960, it is possible to choose I = 40 and M = 32. Similarly, because $I' \times (I' - 1) \times M'/2$ must be at least equal to 1 920, it is possible to choose I' = 24 and M' = 7 (this requires a slight increase in size to 1 932 to facilitate the implementation).

The final size of the memory MM is therefore equal to 26 892 bytes.

The above calculation of I, M, I' and M' for the asymmetrical service A6 can be applied in an analogous manner to the other services of the VDSL system. A table of values for the parameters I, M, I' and M' can therefore be stored in the coding/decoding stage. When the modem is installed at the end of the line, and depending on the service actually provided by the operator, the control means MCD fetch the corresponding values of I, M, I' and M' from the stored table and deliver them to the addressing means MAD1 and MAD2, the structure of which is described in more detail next with reference to figures 7 and 8.

Figure 7 shows that the first addressing means include a first counter CT1 delivering the relative index $\underline{i}$ of a branch BRi at the timing rate of a clock signal. The index $\underline{i}$ is delivered to intermediate calculation means MCI that determine the address adbs of the branch BRi in the first memory space. To be more precise, the address adbs is equal to $\underline{i} \times (\underline{i} - 1)/2$. The means MCI can be easily implemented using multipliers, dividers and subtractors.

The first counter CTI has a counting range equal to I and therefore counts from 0 to I - 1, for example.

The means MD1 further include a second counter CT2

which delivers a current value m equal to the current number of bytes in each block BKj of a branch BRi. The counting range of the counter CT2 is equal to M. In other words, m can vary from 0 to M - 1, for example.

The second counter CT2 is incremented by one unit each time that i = I - 1.

The means MDA1 further include a third counter CT3 which delivers the index j of the block BKj within the branch with index i. The counting range of the counter CT3 is equal to i. In other words, j varies from 0 to i - 1, for example. The third counter CT3 is incremented each time that a block contains M bytes, and therefore in this example each time that the counter CT2 reaches the value M.

The means MDA1 further include first address determination means MD1 which determine the read address ar in the memory and the write address aw in the memory.

To be more precise, the read address ar is equal to (adbs + j) × M + m.

The write address aw is then simply equal to the read address but delayed by one cycle of the clock signal.

Again, the means MD1 can be easily implemented using adders and multipliers.

For example, a small auxiliary dual-port memory with a capacity of (I - 1) × M bits can be used to store the value of the index j delivered by the third counter CT3, which is incremented every M clock cycles. Every M clock cycles, the value of j corresponds to the ith branch in the auxiliary memory, after which the counter CT3 is incremented and the new value is rewritten at the same address.

The second addressing means MDA2 that deliver the read address ar' and the write address aw' in the second memory space of the memory MM have a structure similar to

that just described for the first addressing means MDA1. Only the differences between the means MDA1 and the means MDA2 are described here.

The first counter CT10 delivers the relative index i' of a branch. This time i' varies in the range from I' - 1 to 0. The intermediate calculation means MCI deliver the address of each branch adbs' using a formula analogous to that used to calculate the address, but substituting i' for i.

The second counter CT20 defines the number m' of bytes in a block and is incremented each time that the counter CT10 reaches its counting limit value, in this example when i' reaches the value 0. In this example the second counter CT20 varies in the range from 0 to M' - 1.

The third counter CT30 defines the current index j' of a block in the branch with index i'. It varies in the range from 0 to i' - 1 and is incremented each time that a block contains M' bytes, i.e. when the second counter CT20 reaches the value M'.

The second addressing means MDA2 include second address determination means MD2 which determine the write address aw' and the read address ar'. However, the second address determination means MD2 must allow for the size OF of the first memory space ESM1, which is defined by equation (1) below:

$$OF = I \times (I - 1) \times M/2 \qquad (1)$$

and is stored in a register, for example. For uplink interleaving, the addresses of the memory MM vary in the range from 0 to OF - 1.

The first unoccupied address in the memory MM therefore has the value OF.

The means MD2 then calculate the read address ar' from equation (2) below:

$$ar' = OF + M' \times (adbs' + j') + m' \qquad (2)$$

The write address aw' is equal to the read address and is available on the next clock pulse.

Of course, everything just described here for the terminal TO applies to the terminal TU with deinterleaving means with I branches and interleaving means with I' branches. For the user terminal TU it is then necessary to substitute I' for I, and vice versa, and M' for M, and vice versa, in all of the foregoing description.

It would equally be possible to use a single-port memory in place of a dual-port memory by adopting a clock signal of double the frequency.